

MM54HC237/MM74HC237 3-to-8 Line Decoder With Address Latches

General Description

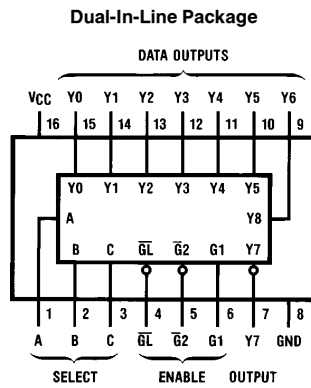
These devices utilize advanced silicon-gate CMOS technology, to implement a three-to-eight line decoder with latches on the three address inputs. When \overline{GL} goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as \overline{GL} remains high no address changes will be recognized. Output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are low unless G1 is high and $\overline{G2}$ is low. The 'HC237 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems.

The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide supply range: 2–6V
- Latched inputs for easy interfacing
- Fanout of 10 LS-TTL loads

Connection Diagram



TL/F/5326-1

Top View

Order Number MM54HC237 or MM74HC237

Truth Table

INPUTS			OUTPUTS										
ENABLE		SELECT											
\overline{GL}	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

H = high level, L = low level, X = irrelevant

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input Voltage (V_{IN})	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		74HC	54HC	Units
						$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of $5V \pm 10\%$ the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC} . The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V, T_A = 25^\circ C, C_L = 15 pF, t_r = t_f = 6 ns$

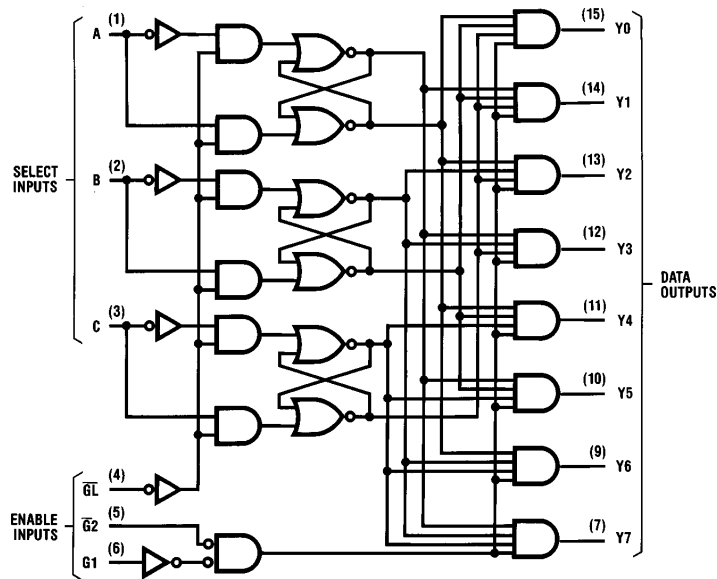
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		20	41	ns
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		16	32	ns
t_{PLH}	Maximum Propagation \overline{GL} to any Y Output		22	44	ns
t_{PHL}	Maximum Propagation Delay \overline{GL} to any Y Output		17	33	ns
t_{PLH}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		16	35	ns
t_{PHL}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		14	25	ns
t_S	Minimum Set Up Time at A, B and C Inputs		10	20	ns
t_H	Minimum Hold Time at A, B and C Inputs		-3	0	ns
t_W	Minimum Pulse Width of Enabling Pulse at \overline{GL}		9	16	ns

AC Electrical Characteristics $C_L = 50 pF, t_r = t_f = 6 ns$ (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		74HC	54HC	Units
						$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	
				Typ	Guaranteed Limits			
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		2.0V	100	235	296	350	ns
			4.5V	24	47	59	70	ns
			6.0V	20	40	50	60	ns
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		2.0V	80	185	233	276	ns
			4.5V	19	37	47	55	ns
			6.0V	17	31	40	47	ns
t_{PLH}	Maximum Propagation \overline{GL} to any Y Output		2.0V	125	250	315	373	ns
			4.5V	25	50	63	75	ns
			6.0V	20	43	54	63	ns
t_{PHL}	Maximum Propagation Delay \overline{GL} to any Y Output		2.0V	95	190	239	283	ns
			4.5V	19	38	48	75	ns
			6.0V	16	32	41	48	ns
t_{PLH}	Maximum Propagation Delay, G1 or $\overline{G2}$ to Output		2.0V	100	200	252	298	ns
			4.5V	20	40	50	60	ns
			6.0V	17	34	43	51	ns
t_{PHL}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		2.0V	73	145	183	216	ns
			4.5V	15	29	37	43	ns
			6.0V	12	25	31	37	ns
t_S	Minimum Set Up Time at A, B and C Inputs		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time at A, B and C Inputs		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of Enabling Pulse at \overline{GL}		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)		75				pF	
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF	

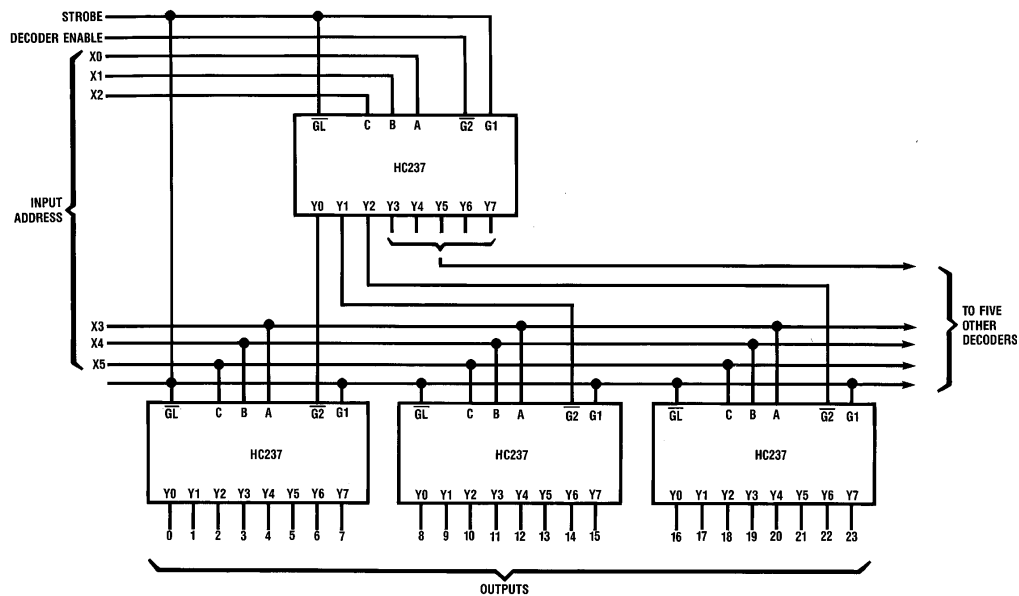
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Functional Block Diagram



TL/F/5326-2

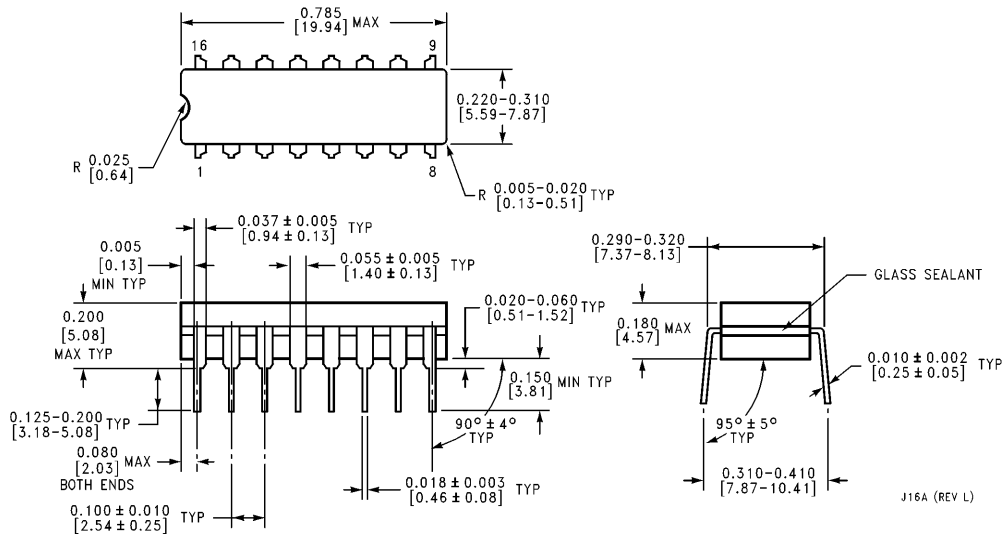
Typical Application



6-Line to 64-Line Decoder with Input Address Storage

TL/F/5326-3

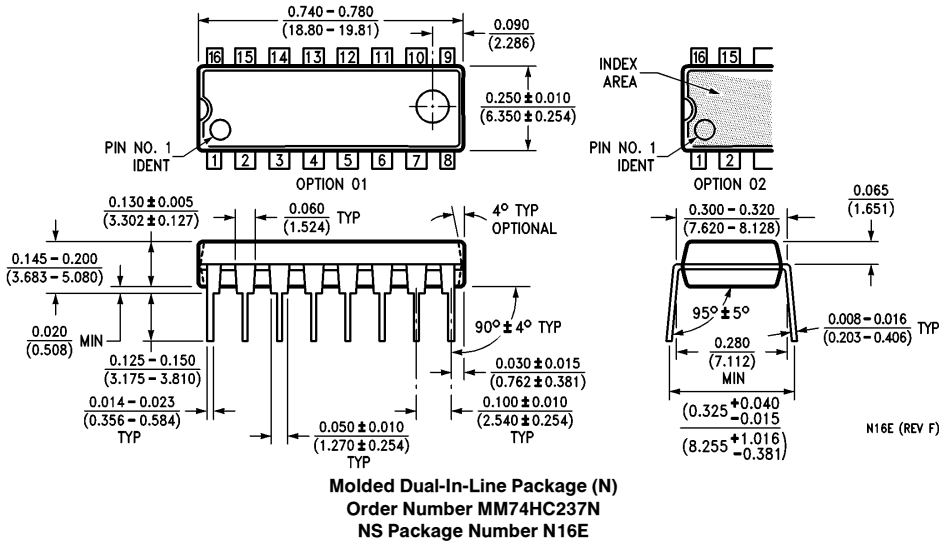
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54HC237J or MM74HC237J
NS Package Number J16A

J16A (REV L)


Physical Dimensions inches (millimeters) (Continued)



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