

MM54HC109A/MM74HC109A Dual J-K Flip-Flops with Preset and Clear

General Description

These J-K FLIP-FLOPS utilize advanced silicon-gate CMOS technology to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

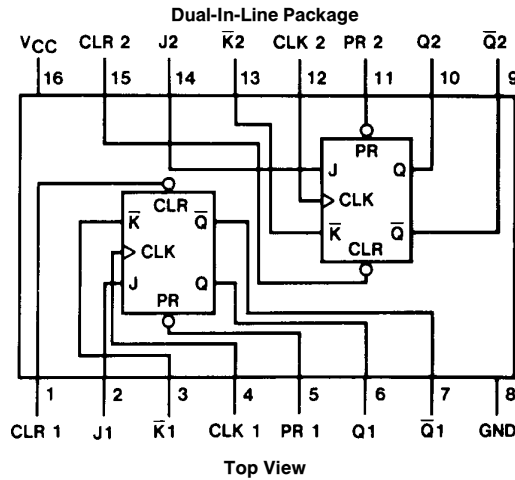
Each flip flop has independent J, \bar{K} PRESET, CLEAR and CLOCK inputs and Q and \bar{Q} outputs. These devices are edge sensitive to the clock input and change state on the positive going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide operating voltage range: 2-6V
- Low input current: 1 μ A maximum
- Low quiescent current: 40 μ A maximum (74HC Series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram



TL/F/5306-1

Order Number MM54HC109A or MM74HC109A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	\bar{K}	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	\uparrow	L	L	L	H
H	H	\uparrow	H	L	TOGGLE	
H	H	\uparrow	L	H	Q0	$\bar{Q}0$
H	H	\uparrow	H	H	H	L
H	H	L	X	X	Q0	$\bar{Q}0$

*This is an unstable condition, and is not guaranteed.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input Voltage (V_{IN})	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$			Units	
				74HC		54HC		
				$T_A = -40$ to $85^\circ C$		$T_A = -55$ to $125^\circ C$		
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA	4.5V		3.98	3.84	3.7	V
			6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA	4.5V		0.26	0.33	0.4	V
			6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of $5V \pm 10\%$ the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC} . The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V, T_A = 25^\circ C, C_L = 15 pF, t_r = t_f = 6 ns$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or \bar{Q}		16	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset or Clear to Q or \bar{Q}		21	42	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			5	ns
t_S	Minimum Setup Time, J or \bar{K} to Clock			20	ns
t_H	Minimum Hold Time, J or \bar{K} to Clock			0	ns
t_W	Minimum Pulse Width: Preset, Clear or Clock		9	16	ns

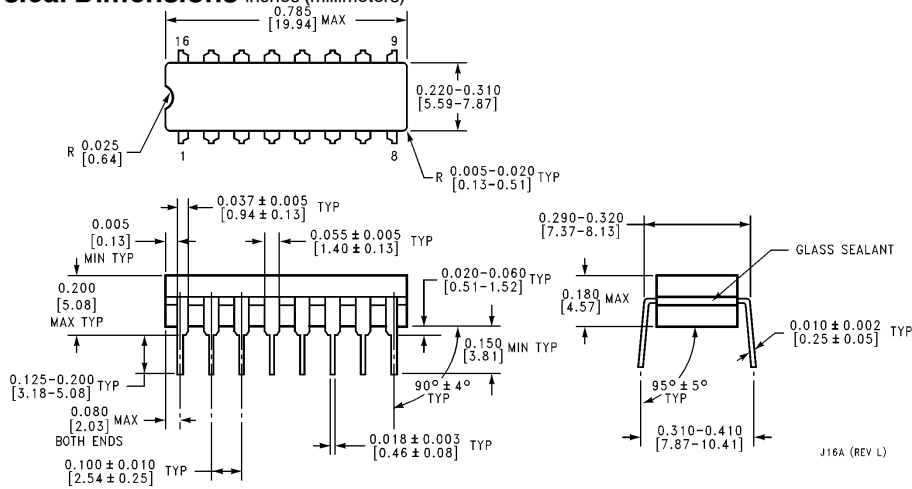
AC Electrical Characteristics $C_L = 50 pF, t_r = t_f = 6 ns$ (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$			Units	
				Typ	74HC $T_A = -40 \text{ to } 85^\circ C$	54HC $T_A = -55 \text{ to } 125^\circ C$		
f_{MAX}	Maximum Operating Frequency		2.0V	5	4	4	MHz	
			4.5V	27	21	18	MHz	
			6.0V	31	24	20	MHz	
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or \bar{Q}		2.0V	88	175	221	ns	
			4.5V	18	35	44	ns	
			6.0V	15	30	37	ns	
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset or Clear to Q or \bar{Q}		2.0V	115	230	290	ns	
			4.5V	23	46	58	ns	
			6.0V	20	39	49	ns	
t_{REM}	Minimum Removal Time Preset or Clear to Clock		2.0V	25	32	37	ns	
			4.5V	5	6	7	ns	
			6.0V	4	5	6	ns	
t_S	Minimum Setup Time J or \bar{K} to Clock		2.0V	100	126	149	ns	
			4.5V	20	25	30	ns	
			6.0V	17	21	25	ns	
t_H	Minimum Hold Time Clock to J or \bar{K}		2.0V	0	0	0	ns	
			4.5V	0	0	0	ns	
			6.0V	0	0	0	ns	
t_W	Minimum Pulse Width Clock, Preset or Clear		2.0V	30	80	100	ns	
			4.5V	9	16	20	ns	
			6.0V	8	14	18	ns	
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V	25	75	95	ns	
			4.5V	7	15	19	ns	
			6.0V	6	13	16	ns	
t_r, t_f	Maximum Input Rise and Fall Time		2.0V	1000	1000	1000	ns	
			4.5V	500	500	500	ns	
			6.0V	400	400	400	ns	
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80			pF	
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

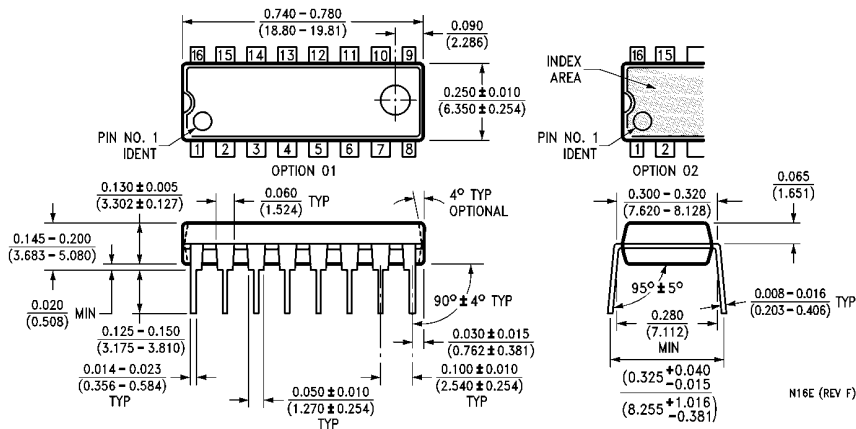
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

MM54HC109A/MM74HC109A Dual J-K Flip-Flops with Preset and Clear

Physical Dimensions inches (millimeters)



**Order Number MM54HC109J or MM74HC109J
NS Package J16A**



**Order Number MM74HC109N
NS Package N16E**

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
19th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.