

# Dual 4-Stage Binary Ripple Counter with $\div 2$ and $\div 5$ Sections High-Performance Silicon-Gate CMOS

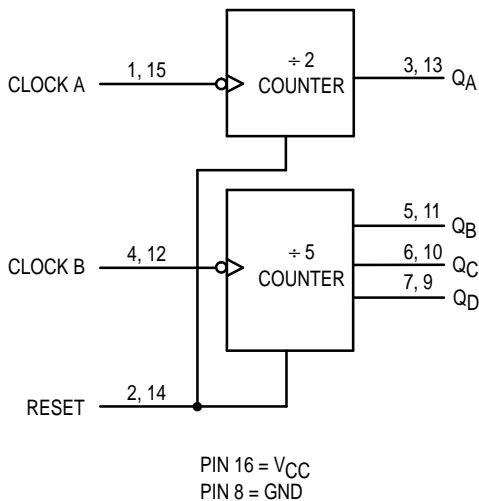
The MC54/74HC390 is identical in pinout to the LS390. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five section. The divide-by-two and divide-by-five counters have separate clock inputs, and can be cascaded to implement various combinations of  $\div 2$  and/or  $\div 5$  up to a  $\div 100$  counter.

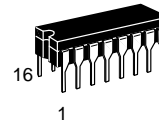
Flip-flops internal to the counters are triggered by high-to-low transitions of the clock input. A separate, asynchronous reset is provided for each 4-bit counter. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or strobes except when gated with the Clock of the HC390.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No 7A
- Chip Complexity: 244 FETs or 61 Equivalent Gates

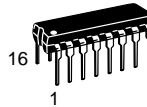
### LOGIC DIAGRAM



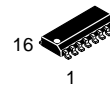
## MC54/74HC390



**J SUFFIX**  
CERAMIC PACKAGE  
CASE 620-10



**N SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08



**D SUFFIX**  
SOIC PACKAGE  
CASE 751B-05

### ORDERING INFORMATION

MC54HCXXXJ	Ceramic
MC74HCXXXN	Plastic
MC74HCXXXD	SOIC

### PIN ASSIGNMENT

CLOCK A <sub>a</sub>	1	16	V <sub>CC</sub>
RESET a	2	15	CLOCK A <sub>b</sub>
Q <sub>Aa</sub>	3	14	RESET b
CLOCK B <sub>a</sub>	4	13	Q <sub>Ab</sub>
Q <sub>Ba</sub>	5	12	CLOCK B <sub>b</sub>
Q <sub>Ca</sub>	6	11	Q <sub>Bb</sub>
Q <sub>Da</sub>	7	10	Q <sub>Cb</sub>
GND	8	9	Q <sub>Db</sub>

### FUNCTION TABLE

Clock		Reset	Action
A	B		
X	X	H	Reset $\div 2$ and $\div 5$
$\sim$	X	L	Increment $\div 2$
X	$\sim$	L	Increment $\div 5$



## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	- 1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic or SOIC DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
Ceramic DIP: - 10 mW/°C from 100° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	- 55	+ 125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				- 55 to 25°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5	3.98	3.84	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
			$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5	0.26	0.33	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	$\mu\text{A}$

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50$  pF, Input  $t_f = t_r = 6$  ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0	5.4	4.4	3.6	MHz
		4.5	27	22	18	
		6.0	32	26	21	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock A to QA (Figures 1 and 3)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock A to QC (QA connected to Clock B) (Figures 1 and 3)	2.0	290	365	435	ns
		4.5	58	73	87	
		6.0	49	62	74	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock B to QB (Figures 1 and 3)	2.0	130	165	195	ns
		4.5	26	33	39	
		6.0	22	28	33	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock B to QC (Figures 1 and 3)	2.0	185	230	280	ns
		4.5	37	46	56	
		6.0	31	39	48	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock B to QD (Figures 1 and 3)	2.0	130	165	195	ns
		4.5	26	33	39	
		6.0	22	28	33	
$t_{PHL}$	Maximum Propagation Delay, Reset to any Q (Figures 2 and 3)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

## NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

CPD	Power Dissipation Capacitance (Per Counter)*	Typical @ 25°C, VCC = 5.0 V			pF
		35			

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**TIMING REQUIREMENTS** (Input  $t_f = t_r = 6$  ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Clock A or Clock B (Figure 2)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
$t_w$	Minimum Pulse Width, Clock A, Clock B (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_w$	Minimum Pulse Width, Reset (Figure 2)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**PIN DESCRIPTIONS**

**INPUTS**

**Clock A (Pins 1, 15) and Clock B (Pins 4, 15)**

Clock A is the clock input to the ÷ 2 counter; Clock B is the clock input to the ÷ 5 counter. The internal flip-flops are toggled by high-to-low transitions of the clock input.

**CONTROL INPUTS**

**Reset (Pins 2, 14)**

Asynchronous reset. A high at the Reset input prevents counting, resets the internal flip-flops, and forces Q<sub>A</sub> through Q<sub>D</sub> low.

**OUTPUTS**

**Q<sub>A</sub> (Pins 3, 13)**

Output of the ÷ 2 counter.

**Q<sub>B</sub>, Q<sub>C</sub>, Q<sub>D</sub> (Pins 5, 6, 7, 9, 10, 11)**

Outputs of the ÷ 5 counter. Q<sub>D</sub> is the most significant bit. Q<sub>A</sub> is the least significant bit when the counter is connected for BCD output as in Figure 4. Q<sub>B</sub> is the least significant bit when the counter is operating in the bi-quinary mode as in Figure 5.

**SWITCHING WAVEFORMS**

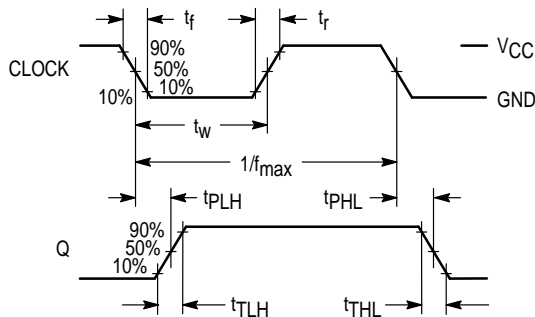


Figure 1.

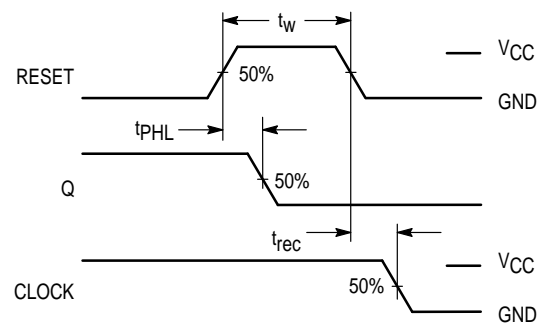
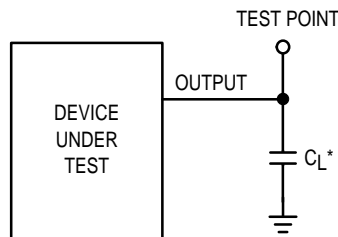


Figure 2.

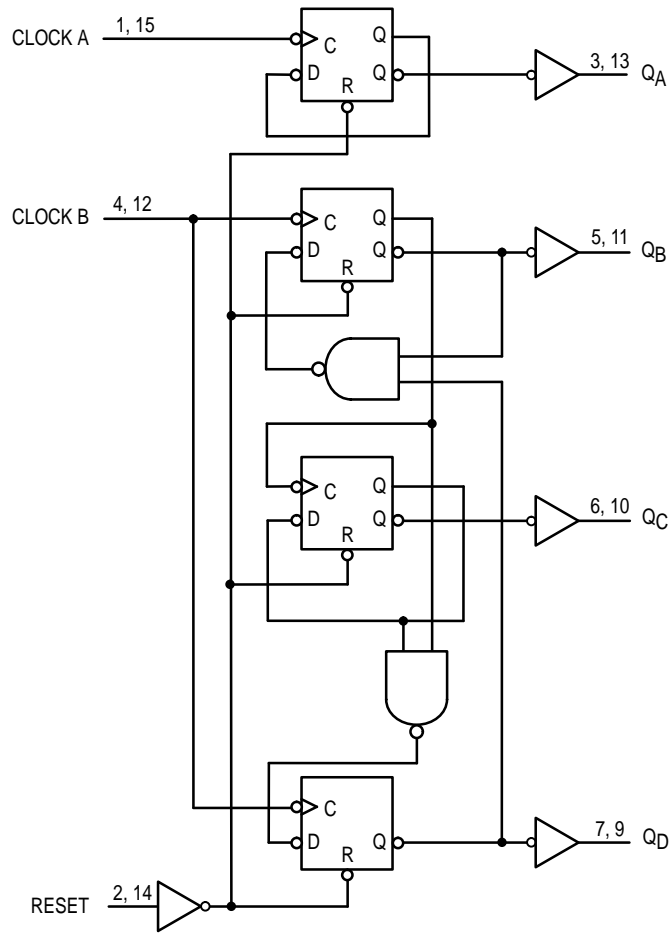
**TEST CIRCUIT**



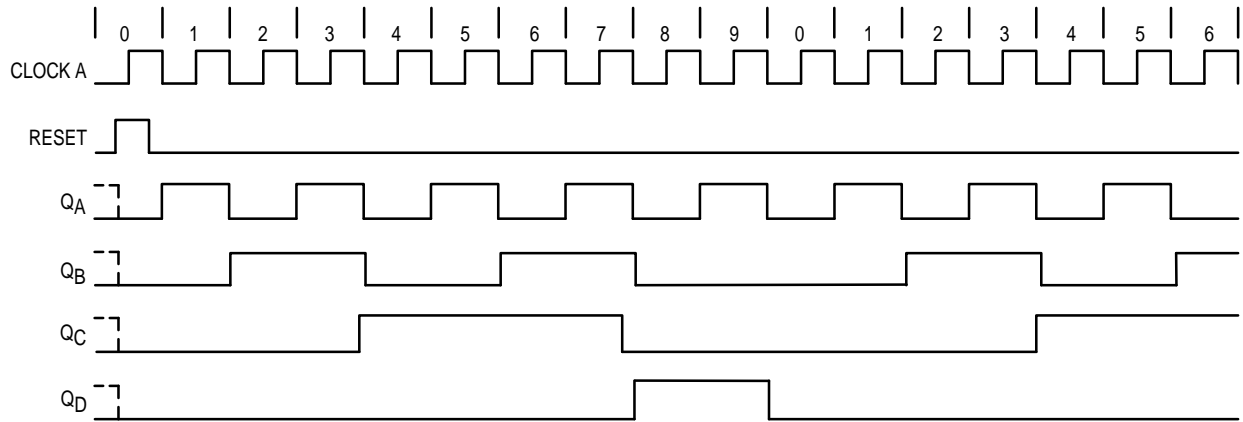
\* Includes all probe and jig capacitance

Figure 3.

**EXPANDED LOGIC DIAGRAM**



**TIMING DIAGRAM  
(Q<sub>A</sub> Connected to Clock B)**



**APPLICATIONS INFORMATION**

Each half of the MC54/74HC390 has independent ÷ 2 and ÷ 5 sections (except for the Reset function). The ÷ 2 and ÷ 5 counters can be connected to give BCD or bi-quinary (2–5) count sequences. If Output Q<sub>A</sub> is connected to the Clock B input (Figure 4), a decade divider with BCD output is obtained. The function table for the BCD count sequence is given in Table 1.

To obtain a bi-quinary count sequence, the input signals connected to the Clock B input, and output Q<sub>D</sub> is connected to the Clock A input (Figure 5). Q<sub>A</sub> provides a 50% duty cycle output. The bi-quinary count sequence function table is given in Table 2.

**Table 1. BCD Count Sequence\***

Count	Output			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

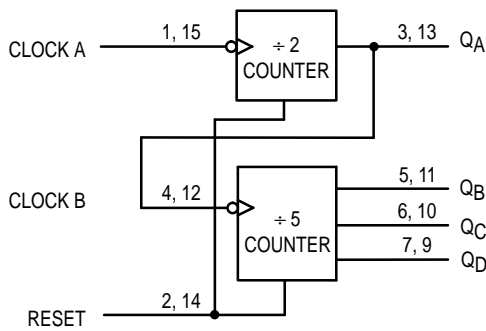
\* Q<sub>A</sub> connected to Clock B input.

**Table 2. Bi-Quinary Count Sequence\*\***

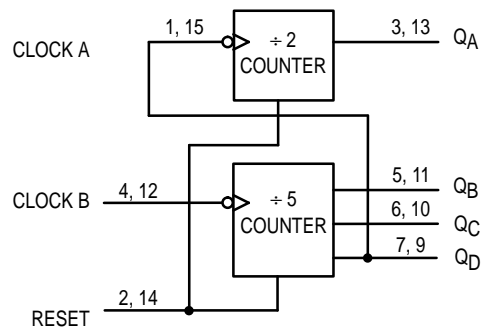
Count	Output			
	Q <sub>A</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L

\*\* Q<sub>D</sub> connected to Clock A input.

**CONNECTION DIAGRAMS**




**Figure 4. BCD Count**



**Figure 5. Bi-Quinary Count**



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