National Semiconductor

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MM54HC166/MM74HC166
8-Bit Parallel In/Serial Out Shift Registers

General Description

The MM54HC166/MM74HC166 high speed 8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER utilizes advanced silicon-gate CMOS technology. It has low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

These Parallel-In or Serial-In, Serial-Out shift registers feature gated CLOCK inputs and an overriding CLEAR input. The load mode is established by the SHIFT/LOAD input. When high, this input enables the SERIAL INPUT and couples the eight flip-flops for serial shifting with each clock pulse. When low, the PARALLEL INPUTS are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high level edge of the CLOCK pulse through a 2-input NOR gate, permitting one input to be used as a clock enable or CLOCK INHIBIT function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. The CLOCK INHIBIT input should be changed to the high level only while the clock input is high. A direct CLEAR input overrides all other inputs, including the CLOCK, and sets all flip-flops to zero.

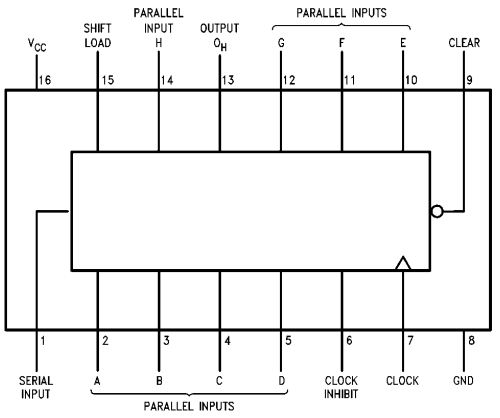
The 54HC/74HC logic family is functionally as well as pin out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and Ground.

Features

- Typical propagation delay:
- Wide operating supply voltage range: 2V–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



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Order Number MM54HC166 or MM74HC166

Function Table

Inputs						Internal Outputs		Output Q_H
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

a . . . h = The level of steady-state input at inputs A through H, respectively

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, Q_H, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Gn} = The level of Q_A, Q_G, respectively, before the most recent ↑ transition of the clock

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40°C to +85°C	54HC T_A = −55°C to +125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND V_{CC} = 2V–6V	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA V_{CC} = 2V–6V	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10%, the worst-case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus, the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V, respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise noted

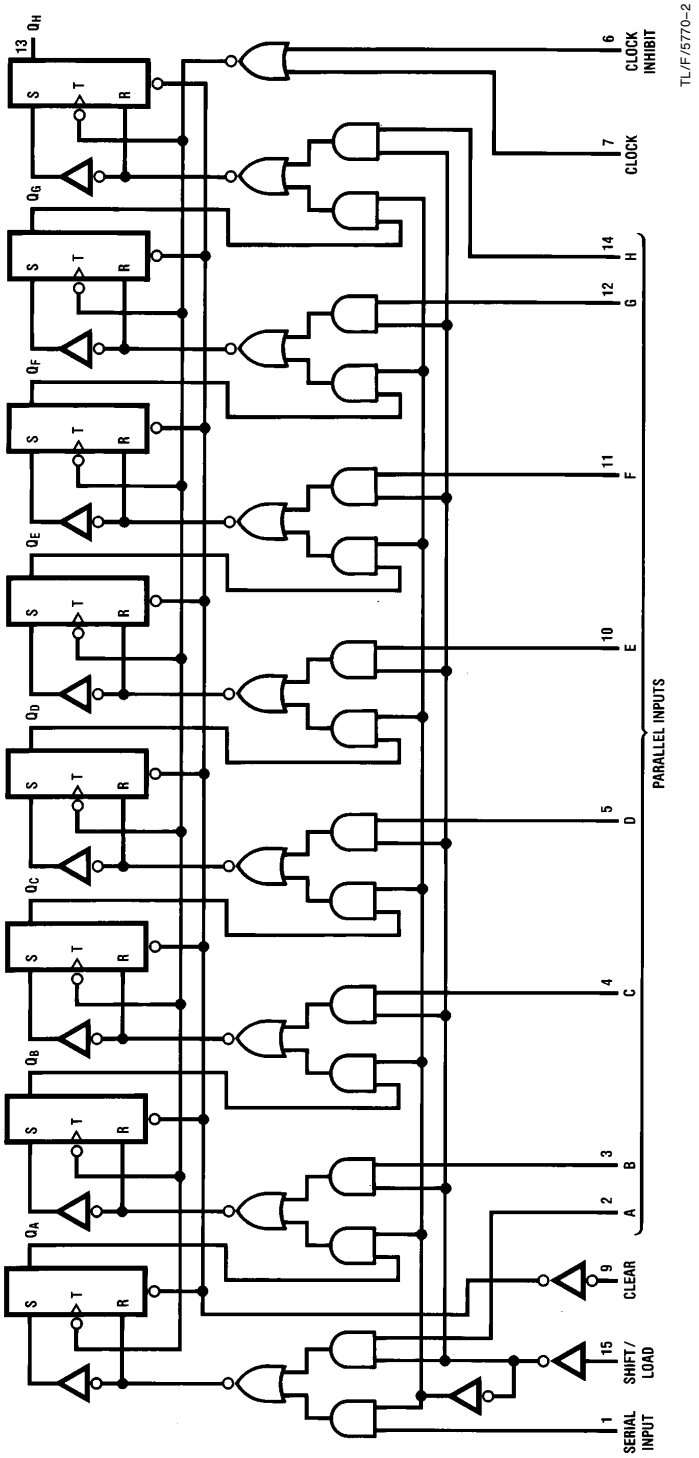
Symbol	Parameter	V_{CC}	$T_A = 25°C$		74HC $T_A = -40°C$ to $+85°C$	54HC $T_A = -55°C$ to $+125°C$	Units
			Typ		Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	2.0V 4.5V 6.0V		6 31 36	5 25 29	4.2 21 25	MHz MHz MHz
t_{PHL}/ t_{PLH}	Maximum Propagation Delay Clock to Q_H	2.0V 4.5V 6.0V	14	140 28 24	175 35 30	210 42 36	ns ns ns
t_{PHL}/ t_{PLH}	Maximum Propagation Delay Clear to Q_h	2.0V 4.5V 6.0V	11	130 26 22	165 35 30	195 39 33	ns ns ns
t_{su}	Minimum Setup Time Shift/Load to Clock	2.0V 4.5V 6.0V		80 16 14	100 20 18	120 24 20	ns ns ns
t_{su}	Minimum Setup Time Data before Clock	2.0V 4.5V 6.0V		80 16 14	100 20 18	120 24 20	ns ns ns
t_{REM}	Minimum Removal Time Clear to Clock	2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_h	Maximum Hold Time Data after Clock	2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_r, t_f	Maximum Output Rise and Fall Time	2.0V 4.5V 6.0V	7	75 15 13	95 19 16	110 22 19	ns ns ns
t_w	Minimum Pulse Width Clock or Clear	2.0V 4.5V 6.0V		80 16 14	100 20 16	120 24 20	ns ns ns
C_{pd}	Power Dissipation Capacitance (Note 5)	(per package)		100			pF
C_{in}	Maximum Input Capacitance		5	10	10	10	pF

AC Electrical Characteristics $V_{CC} = 5V$, $C_L = 15$ pF, $T_A = 25°C$, $t_r = t_f = 6$ ns unless otherwise noted

Symbol	Parameter	Typical	Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		31	MHz
t_{PHL}/ t_{PLH}	Maximum Propagation Delay Clock to Q_h		16	ns
t_{PHL}/ t_{PLH}	Maximum Propagation Delay Clear to Q_h		12	ns
t_{su}	Minimum Setup Time Shift/Load High to Clock		16	ns
t_{su}	Minimum Setup Time Data before Clock		16	ns
t_{REM}	Minimum Removal Time Clear to Clock		0	ns
t_h	Maximum Hold Time Data after Clock		0	ns
t_w	Minimum Pulse Width Clock or Clear		16	ns

Note 5: C_{pd} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



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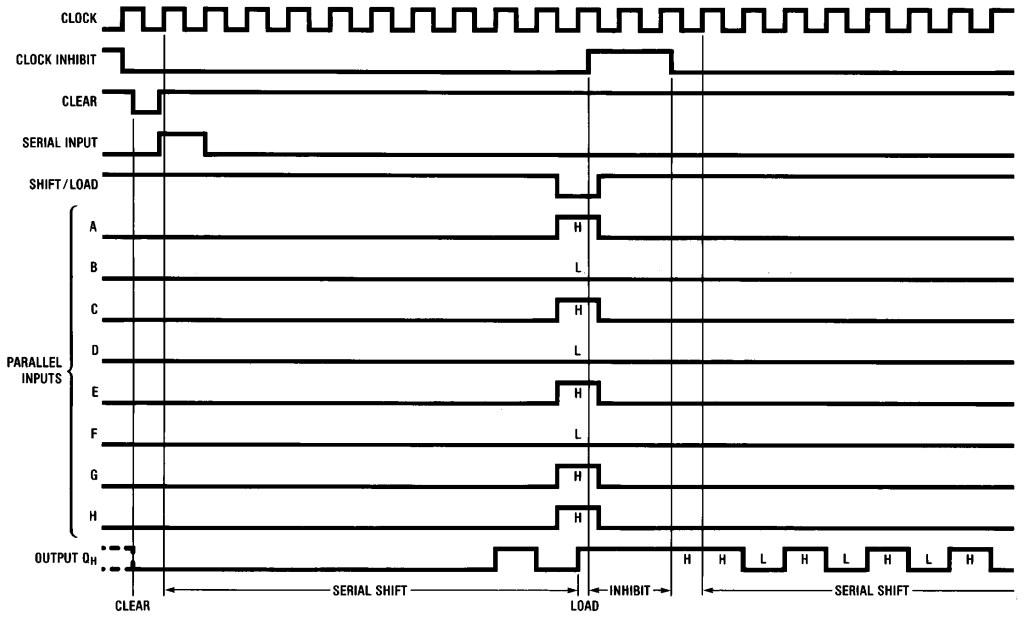
Logic Diagram

Typical Clear, Shift, Load, Inhibit and Shift Sequences



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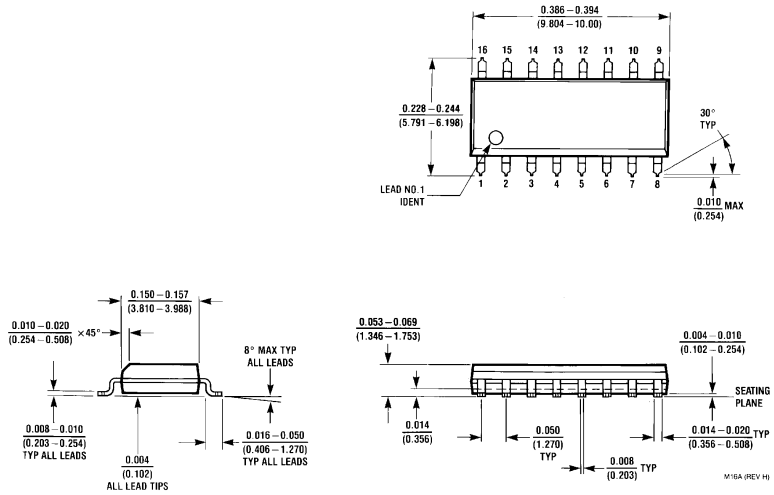
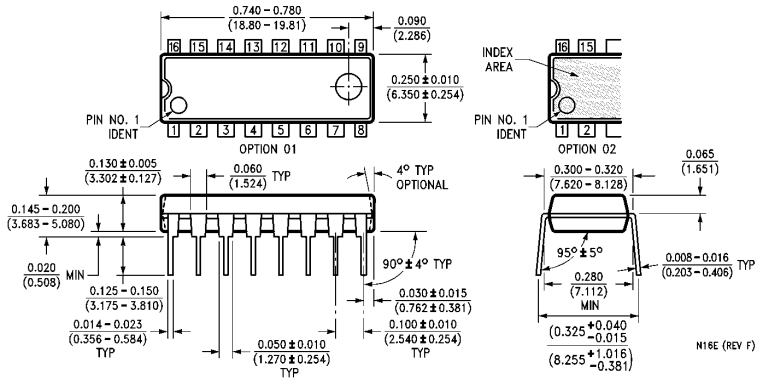
Physical Dimensions inches (millimeters)



Order Number MM54HC166 or MM74HC166
NS Package Number M16A



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