

# HEF40174B

## Hex D-type flip-flop

Rev. 7 — 21 November 2011

Product data sheet

## 1. General description

The HEF40174B is a hex edge-triggered D-type flip-flop with six data inputs (D0 to D5), a clock input (CP), an overriding asynchronous master reset input ( $\overline{\text{MR}}$ ), and six buffered outputs (Q0 to Q5). Information on D0 to D5 is transferred to Q0 to Q5 on the LOW-to-HIGH transition of CP if  $\overline{\text{MR}}$  is HIGH. When LOW,  $\overline{\text{MR}}$  resets all flip-flops (Q0 to Q5 = LOW) independent of CP and D0 to D5.

It operates over a recommended  $V_{\text{DD}}$  power supply range of 3 V to 15 V referenced to  $V_{\text{SS}}$  (usually ground). Unused inputs must be connected to  $V_{\text{DD}}$ ,  $V_{\text{SS}}$ , or another input.

## 2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

## 3. Applications

- Shift registers
- Buffer/storage register
- Pattern generator

## 4. Ordering information

**Table 1. Ordering information**

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

Type number	Package		Version
	Name	Description	
HEF40174BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF40174BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1



### 5. Functional diagram

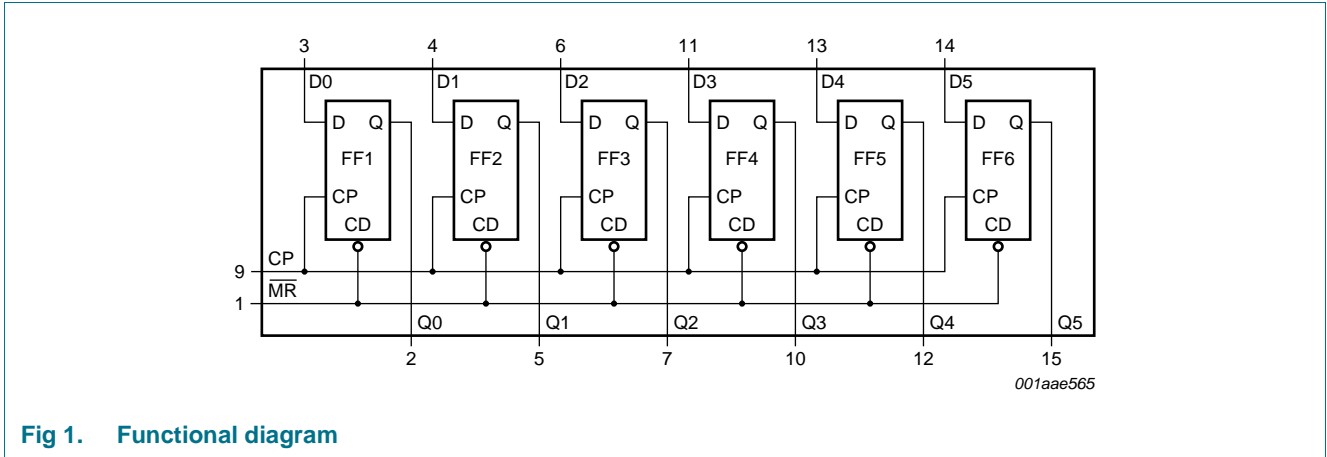


Fig 1. Functional diagram

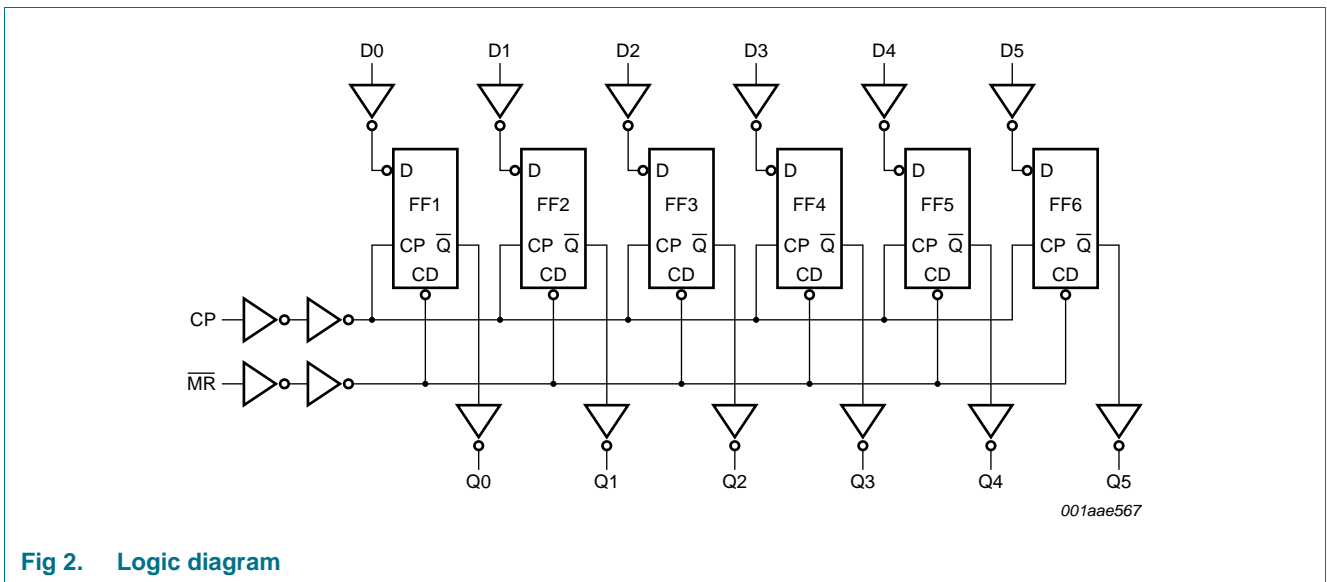


Fig 2. Logic diagram

## 6. Pinning information

### 6.1 Pinning

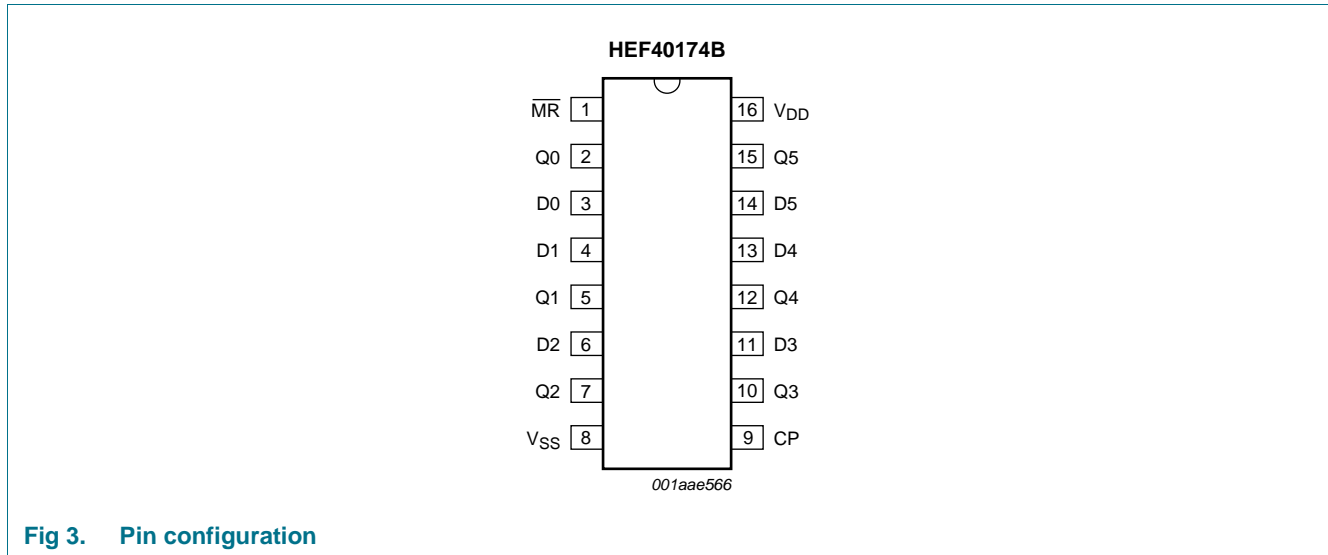


Fig 3. Pin configuration

### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{\text{MR}}$	1	master reset input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5	2, 5, 7, 10, 12, 15	buffered output
D0, D1, D2, D3, D4, D5	3, 4, 6, 11, 13, 14	data input
V <sub>SS</sub>	8	ground supply voltage
CP	9	clock input (LOW-to-HIGH; edge-triggered)
V <sub>DD</sub>	16	supply voltage

## 7. Functional description

Table 3. Function table<sup>[1]</sup>

Input			Output
CP	D	$\overline{\text{MR}}$	Q
↑	H	H	H
↑	L	H	L
↓	X	H	no change
X	X	L	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition.

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DD}$	supply voltage		-0.5	+18	V	
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA	
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V	
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA	
$I_{I/O}$	input/output current		-	$\pm 10$	mA	
$I_{DD}$	supply current		-	50	mA	
$T_{stg}$	storage temperature		-65	+150	°C	
$T_{amb}$	ambient temperature		-40	+85	°C	
$P_{tot}$	total power dissipation	DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
$P$	power dissipation	per output	-	100	mW	

[1] For DIP16 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 10. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V

**Table 6. Static characteristics ...continued**  
 $V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ }^\circ\text{C}$		$T_{amb} = 25\text{ }^\circ\text{C}$		$T_{amb} = 85\text{ }^\circ\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	-	7.5	-	-	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**  
 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; or test circuit see [Figure 5](#); unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	CP to Qn; see <a href="#">Figure 4</a>	5 V	$48\text{ ns} + (0.55\text{ ns/pF})C_L$	-	75	155	ns
			10 V	$19\text{ ns} + (0.23\text{ ns/pF})C_L$	-	30	65	ns
			15 V	$12\text{ ns} + (0.16\text{ ns/pF})C_L$	-	20	45	ns
		$\overline{\text{MR}}$ to Qn; see <a href="#">Figure 4</a>	5 V	$58\text{ ns} + (0.55\text{ ns/pF})C_L$	-	85	175	ns
			10 V	$24\text{ ns} + (0.23\text{ ns/pF})C_L$	-	35	70	ns
			15 V	$17\text{ ns} + (0.16\text{ ns/pF})C_L$	-	25	50	ns
$t_{PLH}$	LOW to HIGH propagation delay	CP to Qn; see <a href="#">Figure 4</a>	5 V	$48\text{ ns} + (0.55\text{ ns/pF})C_L$	-	75	155	ns
			10 V	$19\text{ ns} + (0.23\text{ ns/pF})C_L$	-	30	65	ns
			15 V	$12\text{ ns} + (0.16\text{ ns/pF})C_L$	-	20	45	ns
$t_t$	transition time	see <a href="#">Figure 4</a>	5 V	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
$t_{su}$	set-up time	Dn to CP; see <a href="#">Figure 4</a>	5 V		20	10	-	ns
			10 V		10	5	-	ns
			15 V		10	5	-	ns

**Table 7. Dynamic characteristics ...continued**  
*V<sub>SS</sub> = 0 V; T<sub>amb</sub> = 25 °C; or test circuit see Figure 5; unless otherwise specified.*

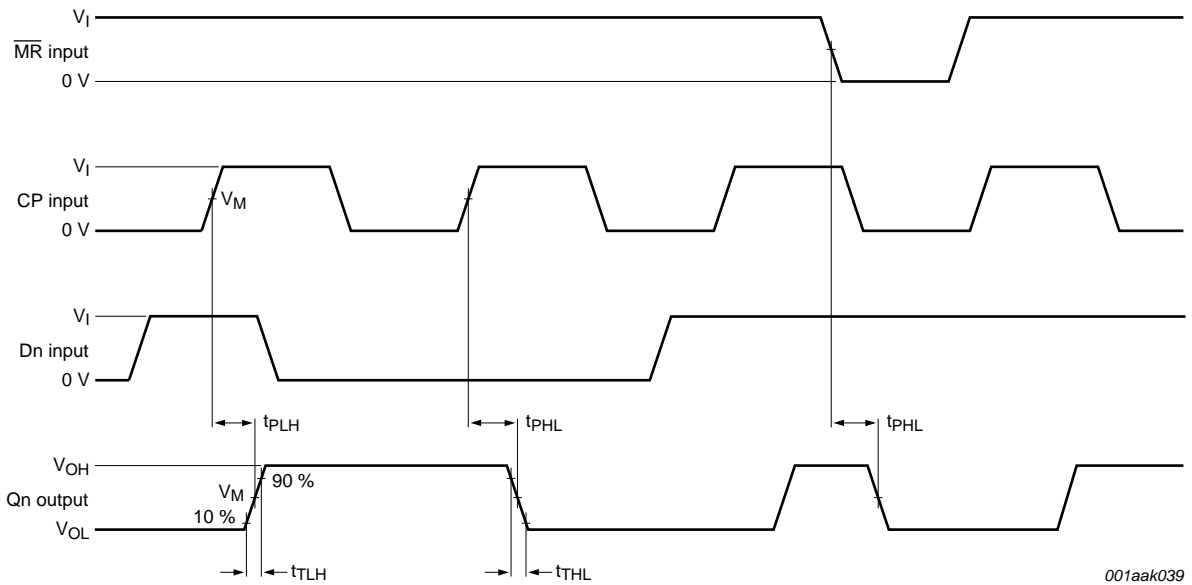
Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula	Min	Typ	Max	Unit
t <sub>h</sub>	hold time	Dn to CP; see Figure 4	5 V		10	0	-	ns
			10 V		5	0	-	ns
			15 V		5	0	-	ns
t <sub>w</sub>	pulse width	CP input LOW; minimum width; see Figure 4	5 V		70	35	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		MR input LOW; minimum width; see Figure 4	5 V		70	35	-	ns
			10 V		35	15	-	ns
			15 V		25	10	-	ns
t <sub>rec</sub>	recovery time	MR input; see Figure 4	5 V		45	25	-	ns
			10 V		20	10	-	ns
			15 V		15	5	-	ns
f <sub>max</sub>	maximum frequency	see Figure 4	5 V		5	11	-	MHz
			10 V		15	30	-	MHz
			15 V		20	45	-	MHz

[1] t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.

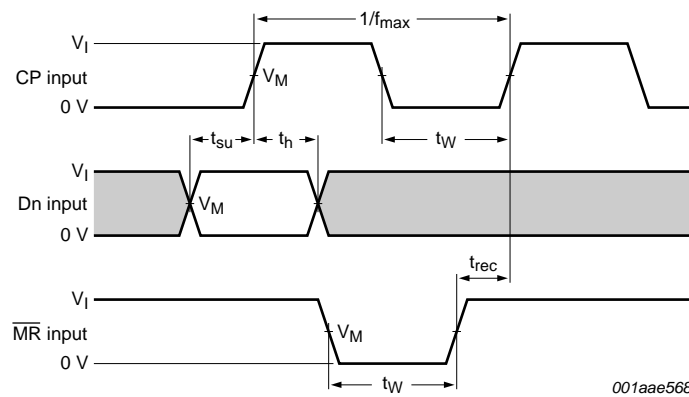
**Table 8. Dynamic power dissipation P<sub>D</sub>**  
*P<sub>D</sub> can be calculated from the formulas shown. V<sub>SS</sub> = 0 V; t<sub>r</sub> = t<sub>f</sub> ≤ 20 ns; T<sub>amb</sub> = 25 °C.*

Symbol	Parameter	V <sub>DD</sub>	Typical formula for P <sub>D</sub> (μW)	where:
P <sub>D</sub>	dynamic power dissipation	5 V	$P_D = 3500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f <sub>i</sub> = input frequency in MHz,
		10 V	$P_D = 16000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f <sub>o</sub> = output frequency in MHz,
		15 V	$P_D = 42000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C <sub>L</sub> = output load capacitance in pF, V <sub>DD</sub> = supply voltage in V, Σ(f <sub>o</sub> × C <sub>L</sub> ) = sum of the outputs.

12. Waveforms



a. CP and  $\overline{MR}$  to Qn Propagation delays and Qn transition times



b. CP and  $\overline{MR}$  minimum pulse widths,  $\overline{MR}$  to CP recovery time, and Dn to CP set-up and hold times

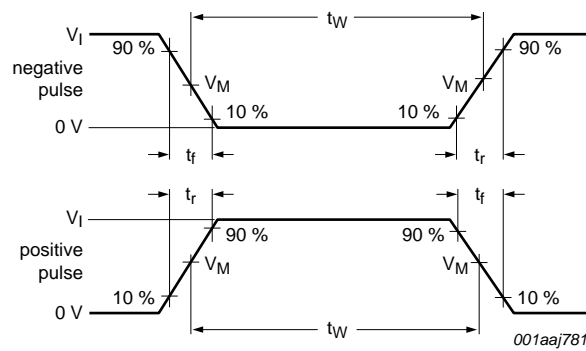
$V_{OH}$  and  $V_{OL}$  are typical output voltage levels that occur with the output load.

Set-up and hold times are shown as positive values but may be specified as negative values.

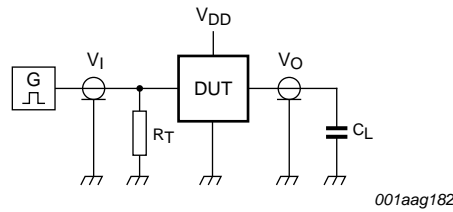
The shaded area are where input changes result in predicable output performance.

Measurement points are given in [Table 9](#).

Fig 4. Waveforms showing switching times



a. Input waveforms



b. Test circuit

Test data is given in [Table 9](#).

Definitions for test circuit:

DUT = Device Under Test

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig 5. Test circuit for measuring switching times

Table 9. Measurement points and test data

Supply voltage	Input			Load
	$V_I$	$V_M$	$t_r, t_f$	$C_L$
5 V to 15 V	$V_{DD}$	$0.5V_I$	$\leq 20$ ns	50 pF



13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

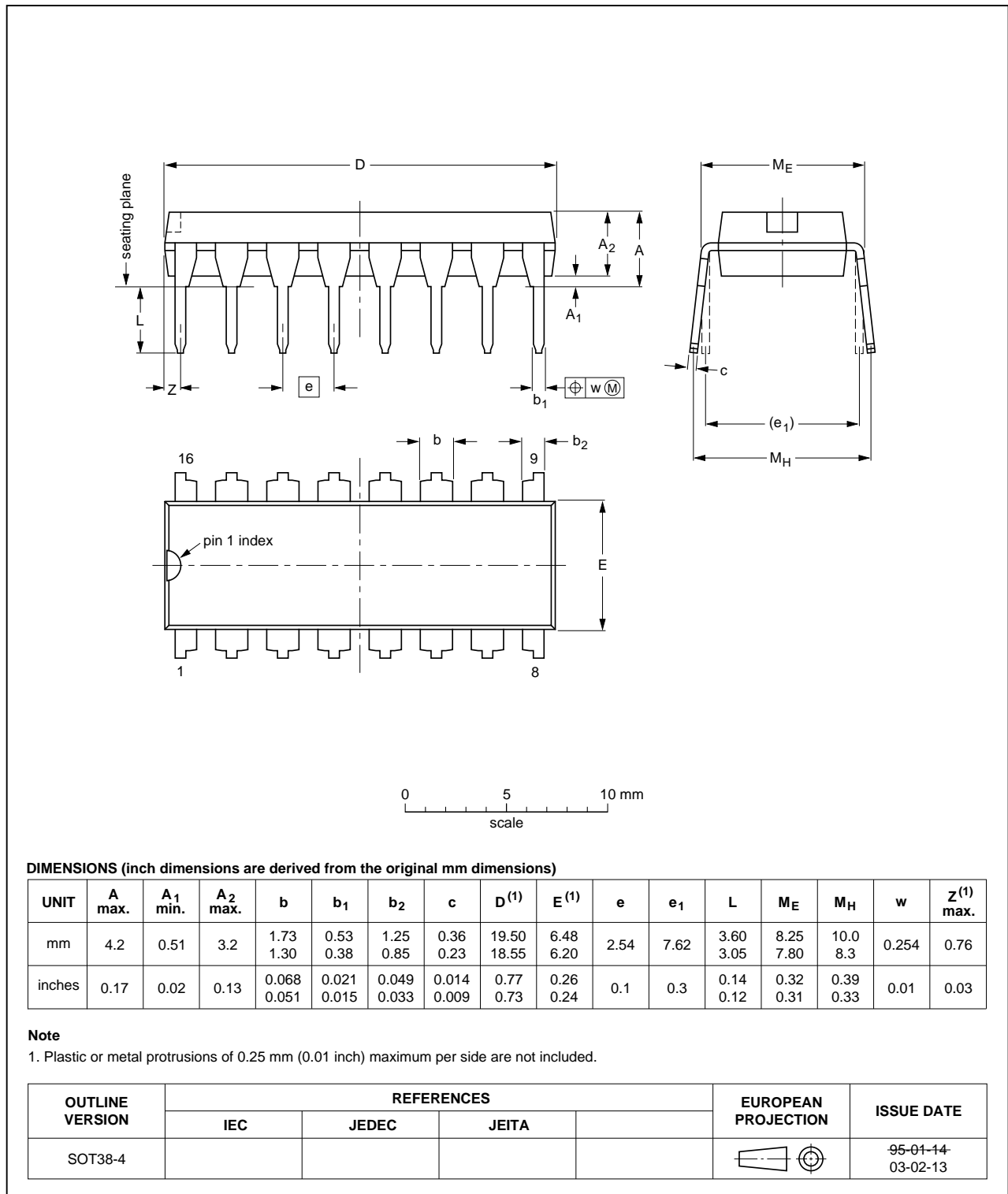


Fig 6. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

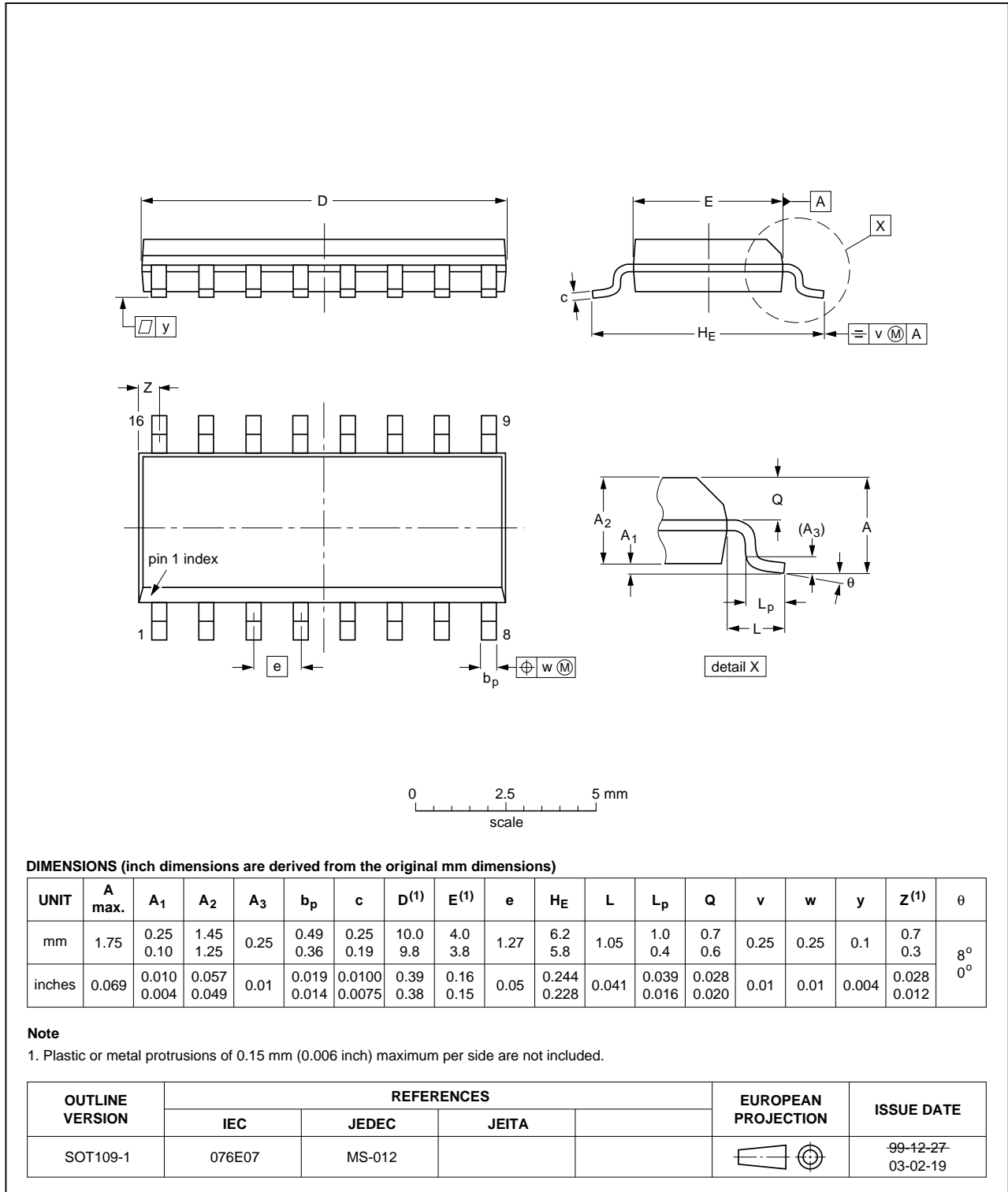


Fig 7. Package outline SOT109-1 (SO16)

## 14. Revision history

**Table 10. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF40174B v.7	20111121	Product data sheet	-	HEF40174B v.6
Modifications:	<ul style="list-style-type: none"><li>• Legal pages updated.</li><li>• Changes in “General description”, “Features and benefits” and “Applications”.</li></ul>			
HEF40174B v.6	20110914	Product data sheet	-	HEF40174B v.5
HEF40174B v.5	20100106	Product data sheet	-	HEF40174B v.4
HEF40174B v.4	20090813	Product data sheet	-	HEF40174B_CNV v.3
HEF40174B_CNV v.3	19950101	Product specification	-	HEF40174B_CNV v.2
HEF40174B_CNV v.2	19950101	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

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Date of release: 21 November 2011

Document identifier: HEF40174B